REMARKS

Applicant has reviewed and considered the Office Action mailed on May 9, 2007, and the references cited therewith.

Claims 27 and 28 have been added, claims 1-8, 17-20, and 22-23 have been amended, and claims 9-16 have been canceled; as a result, claims 1-8 and 17-28 are pending in this application, with claims 1, 17, and 21 being independent.

Claim 7 has been amended to recite "the decision feedback equalizer is configured to automatically iterate the equalization coefficient until the clock and data recovery circuit synchronizes with a frequency of the equalized data." This amendment finds support, for example, on page 7, lines 24-27 of the specification.

Claim 8 has been amended to depend on claim 6 instead of claim 7, and to directly recite a portion of claim 7. Claim 8 has also been amended to recite, "the multiplier is configured to vary the equalization coefficient based on a level of inter-symbol interference in the received data." This amendment finds support, for example, on page 6, lines 24-28 of the specification.

Claim 20 has been amended to recite that the multiplier is "configured to vary the equalization coefficient based on a bit error rate of the received data." This amendment finds support, for example, on page 6, lines 21-33 of the specification.

Claim 27, which has been added and depends on claim 1, recites, "the decision feedback equalizer further comprises a multiplier configured to scale the recovered equalized data by an equalization coefficient, the equalization coefficient being based on a bit error rate of the received data." This claim finds support, for example, on page 6, lines 21-33 of the specification.

Claim 28, which has been added and depends on claim 1, recites, "the decision feedback equalizer further comprises a multiplier coupled to the retimer, the multiplier being configured to apply an equalization coefficient to the recovered equalized data to generate the equalized feedback signal, and the clock and data recovery circuit further comprises a frequency lock detector configured to adjust the equalization coefficient based on a frequency difference exceeding a threshold, the frequency difference being based on a frequency of a reference clock included in the clock and data recovery circuit and a frequency of a divided signal, the divided

signal being generated from the extracted clock signal." This claim finds support, for example, in original claim 7, and on page 9, lines 27-33 and page 10, lines 11-18 of the specification.

Other amendments to the claims and specification have been made to correct matters of form.

OBJECTIONS TO THE DRAWINGS

Figures 1-3 were objected to based on MPEP § 608.02(g) due to their lack of designation as "prior art." Corrected drawings have been filed designating FIGs. 1-3 as "prior art." Accordingly, Applicant respectfully requests that this objection be withdrawn.

The drawings were also objected to under 37 CFR § 1.83(a) on the ground that the drawings do not show a frequency acquisition loop that is configured to adjust a frequency of an extracted clock signal to maintain a fixed relationship between a frequency of a binary signal and a frequency of the extracted clock signal, as recited in pending claims 5, 6, 22, 23, and 26. Applicant respectfully disagrees with this objection on the ground that the drawings, when understood in light of the specification, do show this feature.

FIG. 4 shows a slicer 460, which converts the output of the summer 430 into a binary signal D3. Page 5, lines 31-32. The binary signal output by the slicer 460 drives the data input of a flip flop 470 and a clock and data recovery circuit 420. Page 5, lines 33-35. The clock and data recovery circuit 420 generates an extracted clock signal from the binary signal D3 extracted by the slicer 460. Page 5, line 35 to page 6, line 4.

FIG. 5 shows a block diagram of a clock and data recovery circuit 500, which may be the clock and data recovery circuit 420 shown in FIG. 4. Page 7, lines 22-32. Page 8, lines 12-15 disclose that "the phase lock loop adjusts the phase of the extracted clock to maintain a fixed relationship between the phase of the incoming data signal (e.g. the binary signal (D3) of FIG. 4) and the extracted clock signal." Thus, while FIG. 3 shows the clock and data recovery circuit 320 maintaining a frequency between an extracted clock 330 and incoming data (i.e., a reference signal), FIG. 4 shows the clock and data recovery circuit 420 maintaining a frequency between an extracted clock 430 and a binary signal D3. These disclosures show that the drawings do show the frequency acquisition loop, and Applicant respectfully requests that this objection be withdrawn.

OBJECTION TO THE SPECIFICATION

The Office Action issued an objection to the specification corresponding to the objection to the drawings on the ground that the detailed description does not describe a frequency acquisition loop that maintains a frequency between an extracted clock signal and a binary signal. Applicant respectfully submits that the detailed description does describe such a frequency acquisition loop for the reasons stated above. Accordingly, Applicant respectfully requests that this objection be withdrawn.

§ 112 REJECTIONS

Claims 25 and 26 were rejected under 35 U.S.C. § 112, first paragraph, on the ground that the detailed description does not describe how an equalization coefficient is modified to synchronize the frequencies of the extracted clock signal and the binary signal, as recited in claim 25, upon which claim 26 depends. Applicant respectfully submits that the detailed description does in fact describe how the equalization coefficient is modified.

Page 7, lines 24-30 of the specification discloses that "the equalization coefficient is automatically iterated until the clock and data recovery circuit 420 synchronizes with the frequency of the equalized data at which point a real time optimization loop (not shown) adjusts the equalization coefficient to reduce or minimize the inter-symbol interference in the equalized data." The clock and data recovery circuit 420 generates the extracted clock signal 430. Page 5, line 35 to page 6, line 6. The binary signal D3 is converted from the output of the summer 430, which in turn receives input from the equalized feedback signal 450. Page 5, lines 29-32. Accordingly, the specification does sufficiently describe how the equalization coefficient is modified, and Applicant respectfully requests that this rejection be withdrawn.

§ 103 REJECTIONS

The Office Action rejected claims 1-5, 18, 21, 22, and 24 under 35 U.S.C. § 103(a) as being unpatentable over what the Office Action described as "admitted prior art" in view of Tomita, U.S. Patent No. 6,931,088. Applicant respectfully submits that these rejections were improper because Tomita is improperly applied in the Office Action.

Claim 1, as amended, recites, "the clock and data recovery circuit is configured to generate an extracted clock signal from the equalized data." The Office Action stated that, "[w]ith regard to claims 1-4, 9-12, and 21, the admitted prior art in the present application discloses the claimed invention (see Figure 3; page 1, lines 23-33; and page 3, lines 7-27) except for generating the extracted clock signal from the equalized data. Tomita discloses using an equalized signal to generate the clock for the retimer. (See Figures 1 and 3)."

FIG. 1 of Tomita shows a decision feedback equalizer 12 which reproduces data after storing the data in a shift register 24. Column 1, 56-59. FIG. 1 also shows a timing recovery phase-locked loop 16 which "receives the control signal S7 from the detection circuit 15 and generates a clock signal CLK that is substantially coincident with the phase of the read signal in accordance with the control signal S7." Column 2, lines 4-7. Thus, the clock signal generated by the timing recovery phase-locked loop 16 shown in FIG. 1 generates the clock signal CLK based on the read signal, and not from an equalized signal or data, as recited in claim 1.

FIG. 3 of Tomita shows a decision feedback equalizer 51, a phase-locked loop error detection circuit 53, and a timing recovery phase-locked loop 54. The decision feedback equalizer 51 includes a shift register 63 which outputs the reproduced data. Column 6, lines 27-33. The timing recovery phase-locked loop 54 "generates the clock signal CLK having a phase that is substantially coincident with the phase of the read signal RD." Column 6, lines 55-57. Thus, the clock signal generated by the timing recovery phase-locked loop 54 shown in FIG. 3 also generates the clock signal CLK based on the read signal, and not from an equalized signal or data, as recited in claim 1.

Thus, Tomita does not disclose generating "an extracted clock signal from the *equalized data*" (italics added), as recited in claim 1. Therefore, this element of claim 1 has not been shown, and Applicant respectfully requests that this rejection of claim 1 be withdrawn.

Applicant further requests that the rejections of claims 2-5, which depend on claim 1, be withdrawn based on their dependence on an allowable base claim.

Claim 21 recites, "generating, by the decision feedback equalizer, a binary signal according to the received data; extracting a clock signal from the binary signal." Applicant respectfully requests that the rejection of this claim be withdrawn due to Tomita's failure to disclose extracting a clock signal from a binary signal generated by a decision feedback equalizer, as recited in claim 21, and in similar fashion as discussed above with respect to claim 1.

Applicant requests that the rejection of dependent claim 3 be withdrawn for the further reason that FIG. 3 of the present application does not show, "wherein the clock and data recovery circuit generates the extracted clock signal from the binary signal." The clock and data recovery circuit 320 shown in FIG. 3 (which was relied upon to reject claim 3) generates the extracted clock signal 330 from amplified data D1 which is an amplification of the incoming data. Page 3, lines 11-18. The equalized data D2 output by the slicer 350 is received only by the flip flop 340, and not by a clock and data recovery circuit, as recited in claim 3.

Applicant further requests that the rejections of claims 5, 18, and 22 be withdrawn because the "admitted prior art" is improperly applied in the Office Action. Claims 5 and 18 recite that "the clock and data recovery circuit comprises a frequency acquisition loop and a phase lock loop." Claim 22 recites, "maintaining a fixed frequency relationship between the binary signal and the extracted clock signal by adjusting the frequency of the extracted clock signal; and maintaining a fixed phase relationship between the binary signal and the extracted clock signal by adjusting the phase of the extracted clock signal." The Office Action states that "Figure 5 discloses a 'conventional clock and data recovery circuit' (see page 7, lines 29-30) with a frequency acquisition loop and a phase acquisition loop." However, the entire paragraph beginning on page 7, line 31, reads:

> For example, FIG. 5 is a simplified block diagram of a conventional clock and data recovery circuit 500 *integrated with* a frequency lock detector 510 for generating an extracted clock signal and controlling a real time open loop optimization circuit 590 that generates the equalization coefficient (g1) of the decision feedback equalizer of FIG. 4. In the illustrated embodiment the clock and data recovery circuit includes a frequency

acquisition loop and a phase lock loop. The phase lock loop may operate concurrently or sequentially with the frequency acquisition loop. (Italics added).

Thus, the frequency lock detector 510 and the real time open loop optimization circuit 590 are not "conventional", but are integrated with a "conventional" clock and data recovery circuit. Therefore, Applicant respectfully requests that the rejections of claims 1, 18, and 22 be withdrawn due to the "admitted prior art's" failure to disclose at least these limitations.

The Office Action rejected claims 5-8, 18-20, 22, and 23 as being unpatentable over the "admitted prior art" in view of Tomita and further in view of Kim et al., U.S. Patent No. 6,670,853. Applicant respectfully submits that these rejections are improper for the reasons stated above with regard to claims 1, 17, and 21, upon which claims 5-8, 18-20, and 22-23 respectively depend, and for the further reason that Kim, alone or in combination with the "admitted prior art" and/or Tomita, does not disclose the elements of these claims, as discussed below.

Claims 5 and 18 recite that "[a] clock and data recovery circuit comprises a frequency acquisition loop and a phase lock loop, wherein the frequency acquisition loop adjusts a frequency of the extracted clock signal…and wherein the phase lock loop adjusts a phase of the extracted clock signal." Claim 22 recites, "maintaining a fixed frequency relationship between the binary signal and the extracted clock signal by adjusting the frequency of the extracted clock signal; and maintaining a fixed phase relationship between the binary signal and the extracted clock signal by adjusting the phase of the extracted clock signal." The Office Action states that "Figure 1 of Kim et al. discloses a frequency acquisition loop (110) and a phase acquisition loop (130)." However, the loops of Kim lock the frequency of an internal clock signal INTCK with the frequency of an input signal INS in response to the input signal INS and generates a frequency locking signal FLS, and phase-lock the internal clock signal INTCK with the input signal INS in response to the input signal INS and the internal clock signal INTCK and generates a recovery locking signal RLS. Kim does not disclose adjusting a frequency or phase of an extracted clock signal, as recited in claims 5, 18, and 22. Therefore, Kim, alone or in combination with the "admitted prior art" and/or Tomita, does not disclose at least these elements of the rejected claims. Accordingly, Applicant respectfully requests that the rejections of claims 5, 18, and 22 be withdrawn.

Applicant further requests that the rejections of claims 6-8, 19, 20, and 23, be withdrawn due to their dependence on allowable claims 5, 18, and 22, and due to the amendments to claims 7, 8, and 20, which recite elements not disclosed by the "admitted prior art," Tomita, or Kim, alone or in combination.

Applicant further requests allowance of newly added claims 27 and 28 due to the cited art's failure to disclose the elements of these claims.

Claims 9-16 have been canceled, rendering the rejections of these claims moot. Accordingly, Applicant respectfully requests that the rejections of these claims be withdrawn.

DOUBLE PATENTING REJECTION

Claims 1-4, 9-12, 17, and 21 were provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-4, 7-10, 12, and 22, respectively, of co-pending U.S. Application No. 10/774,725. Claims 9, 10, and 12 have been canceled, rendering these rejections moot, and Applicant respectfully requests that the rejections of these claims be withdrawn.

Applicant has filed a terminal disclaimer in this case, obviating the remaining rejections. Therefore, Applicant respectfully requests that the remaining rejections be withdrawn.

CONCLUSION

Applicant respectfully submits that claims 1-8 and 17-28 are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (208-286-1013) to facilitate prosecution of this application.

No fees are believed to be due at this time. If necessary, please charge any additional fees or credit any overpayment to Deposit Account No. 50-3521, referencing Attorney Docket No. BU3368/0033-115001.

Respectfully submitted,

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208-286-1013

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